## REMARKS

Reconsideration and allowance of the claims of the present application are respectfully requested.

Applicants have corrected the typographical errors in Claims 4 and 5 by replacing the term "aid" in lines 3 and 9 of Claim 4 and the term "aisd" in line 3 of Claim 5 with the word "said". Applicants observe that these amendments to Claims 4 and 5 obviate the objections to Claims 4 and 5 raised in the present Office Action. Thus, the objections to Claims 4 and 5 can and should be withdrawn. Further, applicants have amended Claim 19 by further defining the steps of the claimed method. Support for the amendment to Claim 19 is found in the specification at paragraphs [0021], [0022], [0023], and [0024].

Since the above amendments do not introduce new matter into the application, entry thereof is respectfully requested.

Claims 1-2, 4-8, 11-12 and 17 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S Patent No. 6,846,618 to Hsu, et al. (hereinafter "Hsu et al.").

Applicants respectfully refer to the Declaration pursuant to 37 C.F.R. §1.131 submitted concurrently with the present response, in which the applicants declare that they conceived and reduced to practice the invention, which is disclosed and claimed in the present application, that is directed to a method for processing a semiconductor wafer comprising the steps of (a) etching one or more first regions of a wafer according to a first set of variables, where a remaining portion of said wafer is prevented from being etched; and (b) etching one or more other regions of said remaining portion of said wafer according to another set of etch variables, wherein one or more previously etched first

regions and any remaining portion of said wafer is prevented from being etched, in the United States, prior to August 8, 2002, which is the effective U.S. filing date of Hsu, et al. According to the above-mentioned §1.131 Affidavit, Hsu, et al. is no longer a §102 reference. Therefore, the §102 rejection over Hsu, et al. has been obviated.

Claims 19-20 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S Patent No. 5,994,175 to Gardner, et al. (hereinafter "Gardner et al."). More specifically, the Examiner asserts that Gardner et al. disclose the method for manufacturing the transistor of Claim 19 and the doping variables of Claim 20.

In response, applicants have amended Claim 19 by further defining the steps of the claimed method. Applicants respectfully submit that Claim 19, as amended, is markedly different from the method of Gardner et al.

Gardner et al. disclose a manufacturing process in which semiconductor transistors are fabricated. The substrate disclosed therein typically includes a p-well region and a laterally displaced n-well region. Gardner et al. also teach formation of first and second conductive gates, wherein the first conductive gate is positioned over the p-well region and the second conductive gate is positioned over the n-well region. Gardner et al. further disclose the following steps: an n-channel mask is first formed on the substrate and a first impurity distribution is introduced into the p-well regions; a p-channel mask is then formed on the semiconductor substrate and the a p-type impurity distribution is introduced into the n-well regions and into the second conductive gate structure; next, after removing the p-channel mask (and the n-channel mask), an electrically neutral impurity is introduced into the semiconductor substrate (See Gardner

et al., column 2 lines 45-67 and column 3 lines 1-20 and column 6 line 27 to column 7 line 46).

Notably, according to Gardner et al., the p-channel mask, i.e., the second mask, is formed directly after the introduction of the first impurity distribution. There is no specific teaching in Gardner et al. that the n-channel mask, i.e., the first mask, is stripped prior to the formation of the second mask. To the contrary, Claim 19, as amended, is directed to a method wherein the second layer of photoresist is deposited after stripping the first patterned photoresist. Thus, the method of Claim 19 is different from the method of Gardner et al.

In addition, the present invention minimizes the undesirable etch regionality effects in the lithographic process and improves the wafer yield in semiconductor manufacture, while the Gardner et al. method limits the spreading of the source/drain impurity distributions, thereby decreases the junction depth and increases the sheet resistance of the source/drain regions. Thus, the present invention and the method of Gardner et al. are directed to resolve two substantially different problems.

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates

anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

In view of the above, particularly the different steps of the methods and the different problems to be resolved as a whole, applicants respectfully submit that Claim 19, as amended, and the dependent claim thereof, are not anticipated from the disclosure of Gardner et al. since the applied reference does not teach the claimed method recited in Claim 19. That is, Gardner et al. do not disclose a method that includes: depositing a first layer of photoresist atop a wafer; patterning said first layer of photoresist to expose one or more first regions of said wafer, where remaining portions of said wafer are protected by a first patterned photoresist; doping said wafer in said exposed one or more first regions while a first patterned photoresist protects said remaining portions of said wafer from being doped; stripping said first patterned photoresist; depositing a secondary layer photoresist atop said wafer; patterning said secondary layer of photoresist where said one or more other regions of said wafer is exposed and where said one or more previously doped regions and said any remaining portions of said wafer are protected by a second patterned resist; doping said wafer where said one or more other regions of said wafer is etched while said second patterned resist protects said one or more previously etched regions and said any remaining portions of said wafer from being further doped; and stripping said second patterned photoresist.

The rejections under 35 U.S.C. §102 have been obviated, reconsideration and withdrawal thereof are respectfully requested.

Claim 3 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Hsu, et al. in view of U.S. Patent No. 6,090,717 to Powell, et al. (hereinafter

"Powell et al."). Claims 9-10 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Hsu, et al. in view of U.S. Patent No. 6,716,763 to Li, et al. (hereinafter "Li et al."). Claims 13-16 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Hsu, et al. in view of U.S. Patent No. 4,155,627 to Gale, et al. (hereinafter "Gale et al."). Claim 18 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Hsu, et al. in view of U.S. Patent No. 6,191,046 to Singh, et al. (hereinafter "Singh et al.").

Applicants respectfully submit that, according to the above-mentioned 37 C.F.R. § 1.131 Affidavit, Hsu, et al. is no longer a §102 reference, thereby it can not be relied upon for rejections under 35 U.S.C. §103. Inasmuch as the principle reference spurring each of the obviousness rejections has been removed, the other applied references are further removed from the claimed method as is evident by including those references in rejecting aspects of applicants' dependent claims. None of the other applied references teach or suggest applicants' claimed method comprising the steps of (a) etching one or more first regions of a wafer according to a first set of etch variables, where a remaining portion of said wafer is prevented from being etched; and (b) etching one or more other regions of said remaining portion of said wafer according to another set of etch variables, wherein one or more previously etched first regions and any remaining portion of said wafer is prevented from being etched.

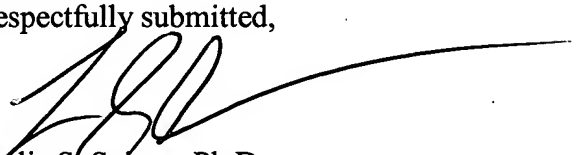
The various 103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include applicants' claimed process in which pre-selected areas of the wafer are treated independently from non-selected areas in a multi-run iterative process. Thus, there is no motivation provided

in the applied references, or otherwise of record, to make the modification mentioned above.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remark, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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